




# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,606	10/24/2003	Robert M. Steinhoff	TI-35706	8813
23494	7590	11/01/2004	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			NGUYEN, CUONG QUANG	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/692,606	Applicant(s) STEINHOFF, ROBERT M.	
	Examiner Cuong Q Nguyen	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.  
     4a) Of the above claim(s) 13-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 12 is/are rejected.
- 7) ☒ Claim(s) 9-11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

## **DETAILED ACTION**

### ***Election/Restriction***

1. Applicant's election without traverse of Group I, claims 1-12 on 08-26-04 is acknowledged.

### **Claim Rejections - 35 USC § 102**

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-8, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ker et al. (US 6,671,153).

Regarding claims 1, 6, 12, Ker et al. discloses a semiconductor device comprising: a voltage node (VDD) coupled to a first p-type region (AR2); a first n-type region (342) having a first side adjoining the first p-type region; a second p-type region (322) having a first side adjoining a second side of the first n-type region; a second n-type region (CR2) having a first side adjoining a second side of the second p-type region; a clamping circuit including a string of diodes (D1, D2 ..., Dn) intercoupled between the second n-type region and a ground VSS); and a switching circuit including

Art Unit: 2811

a MOSFET with a source/drain region intercoupled between the second p-type region and the ground (VSS). See Fig.24A

Regarding claim 4, as shown in Fig.32C, the voltage node comprises a bond pad.

Regarding claims 5 and 7-8, as shown in Fig.25, a switching circuit including a NPN MOSFET with a channel region (323) intercoupled between the second p-type region and a ground (VSS); the switching circuit further comprises a resistor (R3).

### **Claim Rejections - 35 USC § 103**

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art Fig.4 in view of Ker et al. (US 6,671,153).

Regarding claims 1, 5, 12, Admitted prior art Fig.4 Ker et al. discloses a semiconductor device comprising: a voltage node (404) coupled to a first p-type region (408); a first n-type region (412) having a first side adjoining the first p-type region; a second p-type region (410) having a first side adjoining a second side of the first n-type

Art Unit: 2811

region; a second n-type region (414) having a first side adjoining a second side of the second p-type region; a switching circuit including a resistor (418) intercoupled between the second p-type region and a ground (406).

Admitted prior art Fig.4 does not teach that a clamping circuit intercoupled between the second n-type region and ground.

Ker et al. discloses a semiconductor device comprising: a voltage node (VDD) coupled to a first p-type region (AR2); a first n-type region (342) having a first side adjoining the first p-type region; a second p-type region (322) having a first side adjoining a second side of the first n-type region; a second n-type region (CR2) having a first side adjoining a second side of the second p-type region; a clamping circuit including a string of diodes (D1, D2 ..., Dn) intercoupled between the second n-type region and a ground VSS. See Fig.24A

It would have been obvious to one of ordinary skill in the art to form the semiconductor device as shown in admitted prior art Fig.4 including a clamping circuit as taught by Ker et al. in order to form a ESD device without latchup issue. Ker et al.'s col.8 lines 60-64.

Regarding claims 2 and 3, as shown in Admitted prior art Fig.4, a resistor (416) intercoupled between the first n-type region and the voltage node.

### **Allowable Subject Matter**

4. Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for allowance: above references appear to be the closest prior art references. However, these references fail to teach that the clamping circuit comprises a transistor. Prior art of record fails to teach or suggest to incorporate these limitations into above references to arrive at the claimed device.

### **Conclusion**

6. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

7. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

Art Unit: 2811

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Eddie Lee who can be reached on (571) 272-1732.

9. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

A handwritten signature in black ink, appearing to read 'Cuong Nguyen', with a long vertical line extending downwards from the end of the signature.

Cuong Nguyen

Primary examiner

10/26/04